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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,055	12/09/2003	Alexander Roger Deas	22215-00001-US	2982

30678 7590 12/11/2007

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EXAMINER	
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ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,055	DEAS ET AL.	
	Examiner	Art Unit	
	Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 40* is/are pending in the application.

4a) Of the above claim(s) *31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 30, 32 - 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Examine has accepted Applicant's corrections to the Abstract, Drawings, and Specification.

2. Applicant's arguments filed 9/24/2007 have been fully considered but they are not persuasive.

Argument: Applicant has argued that the "first signal" from transmitter 720 is not the same "first signal" that is coupled at the input of the receiver 760 but a signal processed by conventional hybrid circuit 750 and that receiver 760 is not receiver 402 and consequently is not co-located on the same circuit (Remarks 9/24/2007; page 19, last 2 paragraphs).

Response: Examiner respectfully disagrees. Schneider's Fig. 4 shows what Applicant calls the conventional echo-cancellation scheme (Remarks 9/24/2007; page 20, 2nd paragraph). However, Applicant's invention (Fig.1) shows exactly the same type of conventional echo cancellation scheme.

In Schneider Fig. 4, the transmitter 401 and receiver 402 form a transceiver (say, TXRX1). Transmitter 502 and 501 form another transceiver (say TXRX2). In Schneider, transmitter 401 in Fig. 3 corresponds to transmitter 720 in Fig. 4 while receiver 402 corresponds to receiver 760.

- TXRX1 corresponds to the transmitter and receiver on DIE A of Applicant's Fig.1 and TXRX2 correspond to the transmitter and receiver on DIE B of Applicant's Fig. 1.

- In Schneider's Fig. 3, the transmitter of 401 in TXRX1 transmits to receiver 502 in the TXRX2. In Applicant's Fig. 1, the transmitter 10 in DIE A transmits a first signal to the receiver 27 in DIE B (see specification, page 9, lines 22+).

- In Schneider's Fig. 3, the receiver 402 in TXRX1 receives a signal from transmitter 501 in TXRX2. In Applicant's Fig. 1, the receiver 17 in DIE A receives a second signal from the transmitter 20 in DIE B.

- In Schneider, part of the transmitted signal leaks back into receiver 402 via the hybrid 750 and is cancelled by the echo canceller 730. The echo canceller receives as its input the signal from transmitter 401 (or 720). In Applicant's Fig. 1, part of the first signal passes from the transmitter 10 into receiver 17 via the paths comprising 12 and 13. The echo cancellation circuitry receives as it's input the signal from buffer 11.

Argument: Applicant argued that Schneider teaches PAM and therefore implies only amplitude modulation (Remarks 9/24/2007; page 20, 2nd last paragraph).

Response: Schneider also teaches QAM (column7, lines 54 – 59) and therefore both amplitude and phase are modified.

The remaining Applicant's arguments (Remarks 9/24/2007; pages 25 – 39) are based on the above main arguments and therefore the same response is applicable to them.

From the above 4 bullets, it is obvious that the two schemes are very similar and therefore Examiner maintains his rejection as in the previous Office Action.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 6, 16, 35, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984).

Regarding claim 1, Schneider discloses a circuit for point-to-point simultaneous bidirectional high speed signaling to another integrated circuit connected thereto (Fig. 1; column 1, lines 17 –25; column 4, lines 50 - 58), the circuit comprising:

a transmitter for transmitting a first signal to another circuit; (Fig. 1, element 100; Fig. 4, element "Transmitter", column 4, lines 50-58);

a receiver for receiving a second signal from the other circuit, and co-located on the same circuit (Fig. 1, element 100; Fig. 4, element "Receiver", column 4, lines 50-58; column 7,lines 42-43; wherein co-located on the same circuit is interpreted as being in the same transceiver);

wherein the first signal at the output of the transmitter is coupled into the input of the receiver buffer co-locate don the same integrate circuit (Fig. 4, output of the "shaping filter" coupled via the "hybrid" to the "front end");

and a third signal at the input of the transmitter is coupled to the receiver (signal path from output of "precoder" through "echo canceller" to output of the "front end");

wherein the third signal is adjusted in phase and amplitude to cancel the first signal at the output of the receiver buffer, whereby the quality of receiving the second signal is enhanced by canceling echoing of the first signal (Fig. 4, element "echo canceller" and output of the "front end"; column 8, lines 19 – 26; column 1, line 59 – column 2, line 19; wherein the third signal phase and amplitude being adjusted is interpreted as being done by the echo canceller and enhancing the quality of the second signal is interpreted as removing the effect of the crosstalk that is troublesome).

Schneider does not disclose that the transceivers are on integrated circuits, differential signaling and that differential buffers are used for coupling the transmitter and receiver and for the echo canceller.

In the same field of endeavor, however, Ambrosio discloses an echo canceller for bidirectional transmission that is implemented on an integrated circuit (column 2, lines 15 – 16).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Ambrosio, in the system of Schneider because this would allow the echo canceller to be implemented on an integrated circuit, thereby reducing the cost and size, as is well known in the art.

In the same field of endeavor, however, Adham discloses a differential buffer that can be used as the transmit buffer, the receive buffer, to couple the input of the transmitter buffer and the output of the receiver buffer, to couple the third signal to the output of the receive buffer, and to couple the transmitter to the receiver (Fig. 1A, column 5, line 59 – column 6, line 25).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Adham, in the system of Schneider because this would allow the echo canceller to be implemented using differential buffers (amplifiers), thereby simplifying the design, reducing crosstalk, having a high SNR, as stated by Adham (column 6, lines 39 – 47).

Regarding claim 4, Schneider does not disclose that the differential buffer is implemented as a chain of buffer stages.

In the same field of endeavor, however, Adham discloses the differential buffer is implemented as a chain of buffer stages (Fig. 5A; column 9, lines 7 – 21).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Adham, in the system of Schneider because this would allow the degraded signals to be restored after a few logic stages, as stated by Adham.

Regarding claim 6, Schneider does not disclose that the differential buffer has a variable current source.

In the same field of endeavor, however, Adham discloses the differential buffer has a variable current source for the purpose of setting the amplitude or phase of the third signal (column 5, line 59 – 67; column 6, lines 6 – 25; wherein setting the amplitude is interpreted as changing the voltage drop across the resistor).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Adham, in the system of Schneider because this would allow the output to be calculated utilizing the benefits of a differential buffer, namely reducing crosstalk, having a high SNR, as stated by Adham (column 6, lines 39 – 47).

Regarding claim 16, Moore discloses the coarse delay circuit is cascaded with the fine delay circuit to produce a delay circuit with a wide range and high resolution (Fig. 1, elements 11 and 12).

Claim 35 is directed to method/steps of the same subject matter claimed in apparatus claim 1 and therefore, is rejected as explained in the rejection of claim 1.

Regarding claim 37, Moore does not disclose that the rise time of the third signal is adjusted to match the rise time of the first signal.

In the same field of endeavor, however, Geist discloses the rise time of the third signal applied to the output of the receiving buffer is adjusted to match the rise time of the first signal (Abstract; Fig. 3; column 3, lines 36 – 51; wherein the third signal is interpreted as the signal A#40 that is adjusted to match the slope of the other signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the combined system of Schneider, Adham and Ambrosio because it would enable the two signals to be synchronized, thereby eliminating any off center crossing voltages, as disclosed by Geist (column 1, lines 32 – 45).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Geist (US 6,362,672).

Regarding claim 2, the combined system of Schneider, Adham and Ambrosio does not disclose that the third signal is adjusted in rise time.

In the same field of endeavor, however, Geist discloses the third signal is further adjusted in rise time (Abstract; Fig. 3; column 3, lines 36 – 51; wherein the third signal is interpreted as the signal A#40 that is adjusted to match the slope of the other signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the combined system of Schneider, Adham and Ambrosio because it would enable the two signals to be synchronized, thereby eliminating any off center crossing voltages, as disclosed by Geist (column 1, lines 32 – 45).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Bellenger (US 6,320,867).

Regarding claim 3, the combined invention of Schneider, Adham and Ambrosio does not disclose that a training pattern is used to adjust the amplitude and phase during power or on request.

In the same field of endeavor, Bellenger discloses the phase and/or amplitude of the third signal is adjusted by applying a training pattern (column 27, lines 59 – column 29, line 3; wherein the third signal is interpreted as the echo replica, adjusting the phase/amplitude is interpreted obtaining the echo canceller coefficients using the training sequence).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of Schneider because this would provide a means for training the echo canceller, as is well known in the art.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Minami et al. (US 4,977,551).

Regarding claim 5, Schneider does not disclose that the finite state machine reads the value from a peak detector and setting a value that controls the current sources in the differential buffer.

In the same field of endeavor, however, Minami discloses the finite state machine employs a peak detector and means of reading a parameter related to the peak detector to set a value through digital to analogue converters (column 2, lines 35 – 49; wherein the finite state machine is interpreted as the control unit).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Minami, in the system of Schneider because this would provide a means for adjusting the tracking signal (Minami; column 2, lines 30-31).

In the same field of endeavor, however, Adham discloses controlling the currents sources in the differential stages in the chain of buffers providing the third signal between the transmitter and receiver (column 5, lines 64 – 67; wherein the controlling the current sources is interpreted as setting the voltage on terminal 10b).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Adham, in the system of Schneider because this would provide a means for adjusting the gain of the differential amplifier, as is well known in the art.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Bellenger (US 6,320,867) and Chang et al. (A CMOS Differential Buffer Amplifier with Accurate Gain and Clipping Control; July 1995, IEEE Journal of Solid State Circuits; pages 731 – 735).

Regarding claim 7, Schneider does not disclose that the gain of the differential buffer is varied by a training pattern.

In the same field of endeavor, however, Chang discloses the programmable or variable load is set by means of a finite state machine (page 731, 2nd column, 6 lines starting with "However, for modern digital telephone applications, ..."; wherein the finite state machine that controls the gain is interpreted as the external gain control).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Chang, in the system of Schneider because allowing the gain to be externally controlled would allow greater flexibility, as is well known in the art.

In the same field of endeavor, however, Bellenger discloses a training pattern (column 24, lines 52 – 67; Fig. 9).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of Schneider because this would allow the echo canceller to be initialized during the training period, as is well known in the art.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomasson (US 6,278,785) and Geist (US 6,362,672).

Regarding claim 8, the combined system of Schneider, Adham and Ambrosio does not disclose a coarse delay circuit, a fine delay circuit, an amplitude control circuit and a rise-time control circuit.

In the same field of endeavor, however, Moore discloses a coarse delay circuit and a fine delay circuit (Abstract; Fig. 1, elements 11, 12; column 1, lines 10 – 21; column 2, lines 5 – 21, 44 – 50).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Moore, in the combined system of Schneider, Adham and Ambrosio because this would provide a means for adjusting the delay for echo cancellation, as disclosed by Moore (column 1, lines 10 – 21).

In the same field of endeavor, however, Thomasson discloses an amplitude control circuit (Abstract; Fig. 1, element 41; column 3, lines 60 – 65; column 5, lines 24 – 33).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Thomasson, in the combined system of Schneider, Adham and Ambrosio because this would provide a means for adjusting the amplitude of the echo replica for echo cancellation, as disclosed by Thomasson.

In the same field of endeavor, however, Geist discloses a rise-time control circuit (Abstract; Fig. 3; column 1, lines 5 – 8; column 3, lines 36 – 51).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the combined system of Schneider, Adham and Ambrosio because it would enable the two signals to be synchronized, thereby eliminating any off center crossing voltages, as disclosed by Geist (column 1, lines 32 – 45).

11. Claims 9, 14, 15, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785), Geist (US 6,362,672) and Bellenger (US 6,320,867).

Regarding claim 9, the combined invention of Schneider, Adham, Ambrosio, Moore and Thomasson does not disclose that a training pattern is used to adjust the amplitude, phase and rise-time during power or on request.

In the same field of endeavor, Bellenger discloses the phase and/or amplitude of the third signal is adjusted by applying a training pattern (column 27, lines 59 – column 29, line 3; wherein the third signal is interpreted as the echo replica, adjusting the phase/amplitude is interpreted obtaining the echo canceller coefficients using the training sequence).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of

Schneider because this would provide a means for training the echo canceller, as is well known in the art.

In the same field of endeavor, Geist discloses the rise-time is adjusted (Abstract; Fig. 3; column 3, lines 36 – 51; wherein the third signal is interpreted as the signal A#40 that is adjusted to match the slope of the other signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the system of Schneider, Adham, Ambrosio, Moore and Thomasson because this would provide a means for matching the rise times in the two signals.

Regarding claim 14, Moore discloses a finite state machine generates control signals to select the signals from the digital delay line in the coarse delay circuit varying the delay of the third signal with respect to the first signal (Fig. 2, elements 16 and r_n; column 2, lines 51 – 67; wherein the controls signals that are generated to select delays from the delay line are interpreted as the read and write pointers).

Regarding claim 15, Moore discloses a finite state machine generates control signals to select the signals from the delay circuits in the fine delay circuit varying the delay of the third signal with respect to the first signal (Fig. 2, elements 16 and r_n; column 2, lines 51 – 67; wherein the controls signals that are generated to select delays from the delay line are interpreted as the read and write pointers; column 3, line 66 – column 4, line 8).

Regarding claim 20, the combined invention of Schneider, Adham, Ambrosio, Moore, Thomasson and Bellenger does not disclose the rise time control circuit comprises resistors, capacitors and switches.

In the same field of endeavor, Geist discloses the rise time control circuit comprises resistors, capacitors and switches (Abstract; Fig. 3, 5; column 3, lines 36 – 51; wherein the resistors and capacitors are as shown in Fig. 5).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the combined system because this would provide a means for matching the rise times in the two signals.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785), Geist (US 6,362,672), Bellenger (US 6,320,867) and Minami et al. (US 4,977,551).

Regarding claim 10, the combined invention of Schneider, Adham, Ambrosio, Moore, Thomasson and Geist does not disclose a peak error detector is used and a parameter is use to set the amplitude, phase and rise-time of the third signal.

In the same field of endeavor, however, Minami discloses the finite state machine employs a peak detector and means of reading a parameter related to the peak

detector, the parameter being used to set a value through a digital to analogue converter (column 2, lines 35 – 49; wherein the finite state machine is interpreted as the control unit).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Minami, in the combined system described above because this would provide a means for adjusting the tracking signal (Minami; column 2, lines 30-31).

In the same field of endeavor, Bellenger discloses the phase and/or amplitude of the third signal is adjusted (column 27, lines 59 – column 29, line 3; wherein the third signal is interpreted as the echo replica, adjusting the phase/amplitude is interpreted obtaining the echo canceller coefficients using the training sequence).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of Schneider because this would provide a means for training the echo canceller, as is well known in the art.

In the same field of endeavor, however, Geist discloses the third signal is further adjusted in rise time (Abstract; Fig. 3; column 3, lines 36 – 51; wherein the third signal is interpreted as the signal A#40 that is adjusted to match the slope of the other signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the combined system

of Schneider, Adham and Ambrosio because it would enable the two signals to be synchronized, thereby eliminating any off center crossing voltages, as disclosed by Geist (column 1, lines 32 – 45).

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785) and Geist (US 6,362,672).

Regarding claim 11, Moore discloses coarse delay circuit comprises a digital delay line and control logic for controlling the multiplexers (Fig. 2; column 2, lines 51 – 67; wherein the control logic for controlling the multiplexers is interpreted as the control logic for the write pointer 16 and read pointer r_n).

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785), Geist (US 6,362,672), Bellenger (US 6,320,867) and Saeki (US 20020070783).

Regarding claim 12, the combined invention of Schneider, Adham, Ambrosio, Moore, Thomason, Geist and Bellenger does not disclose that the digital delay line comprises a cascade of buffers.

In the same field of endeavor, however, Saeki discloses the digital delay line comprises a cascade of buffers (Fig. 18, element 14; page 1, paragraph 3).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Saeki, in the combined system described above because this would provide a means for storage of the signal, as is well known in the art.

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785), Geist (US 6,362,672), Bellenger (US 6,320,867) and Nourrcier (US 5,278,567).

Regarding claim 13, the combined invention of Schneider, Adham, Ambrosio, Moore, Thomason, Geist and Bellenger does not disclose a pair of multiplexers selects signals from a digital delay line.

In the same field of endeavor, however, Nourrcier discloses a pair of multiplexers selects signals from a digital delay line (Fig. 7; column 9, line 67 – column 10, line 24)..

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Nourrcier, in the combined system described above because this would provide selecting the delay line signal, as is well known in the art.

16. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Thomason (US 6,278,785).

Regarding claim 17, Moore does not disclose the finite state machine plus ADC generates a control voltage to vary the amplitude of the third signal.

In the same field of endeavor, however, Thomasson discloses the finite state machine plus ADC generates a control voltage to vary the amplitude of the third signal (Fig. 1, element 41, output of element 42; column 2, lines 17 – 21; wherein the control voltage is interpreted as output of the subtractor 42 that is fed back to change the variable attenuator 41 which changes the amplitude of the echo replica signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Thomasson, in the system of Moore because this would allow the amplitude of the echo replica signal to be controlled for echo cancellation, as is well known in the art.

17. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785), Geist (US 6,362,672) and Filliman et. al. (US 6,404,255).

Regarding claim 18, the combined invention of Schneider, Adham, Ambrosio, Moore, Thomason and Geist does not disclose the amplitude control circuit comprises a buffer with variable load.

In the same field of endeavor, however, Filliman discloses the amplitude control circuit comprises a buffer with variable load (Fig. 7; column 6, line 42 – column 7, line 8).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Filliman, in the combined system because this would allow the amplitude of the echo replica signal to be controlled for echo cancellation, as is well known in the art.

18. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785), Geist (US 6,362,672), Filliman et. al. (US 6,404,255) and Marbot (US 5,334,891).

Regarding claim 19, the combined invention of Schneider, Adham, Ambrosio, Moore, Thomason, Geist and Filliman does not disclose the transistors are NMOS transistors.

In the same field of endeavor, however, Marbot discloses the transistors are NMOS transistors (Fig. 1; column 2, lines 10 – column 3, line 14).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the NMOS transistors, as taught by Marbot, in the combined system because this would result in low power consumption , as is well known in the art.

19. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Moore et al. (US 6,166,573), Thomason (US 6,278,785), Geist (US 6,362,672), Bellenger (US 6,320,867) and Julstrom (US 4,991166).

Regarding claim 21, the combined invention of Schneider, Adham, Ambrosio, Moore , Thomasson, Geist and Bellenger does not disclose that the rise time is controlled by the capacitor.

In the same field of endeavor, however, Julstrom discloses a finite state machine generates control signals to switch the capacitors in the rise-time control circuit varying

the rise-time of the third signal (column 9, lines 49 – 63; wherein the rise time is controlled by the capacitors).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Julstrom, in the combined system because this would allow the rise time to be adjusted.

20. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Michalik (US 4,644,178) and Eisenberg (US 5,742,201).

Regarding claim 22, Schneider does not disclose the peak detector comprises an amplitude cancellation sensor and a phase cancellation sensor and a mux.

In the same field of endeavor, however, Michalik discloses the peak detector comprises an amplitude cancellation sensor (Fig. 1; element 12; column 3, lines 18 – 31; wherein the amplitude cancellation sensor is interpreted as the amplitude sensor 12).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Michalik, in the system of Schneider because this would provide a means for detecting the peak of the signals provided by the sensor, as is disclosed by Michalik.

In the same field of endeavor, however, Eisenberg discloses the peak detector comprises a phase cancellation sensor (Fig. 17; column 11, lines 55 – 65; wherein the phase cancellation sensor is interpreted as the phase detector).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Eisenberg, in the system of Schneider because this would provide a means for detecting the phase of signals, as is disclosed by Eisenberg.

21. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Pandula (US 5,559,841).

Regarding claim 23, Schneider does not disclose the phase cancellation sensor comprises a full wave rectifier, integrator and sample and hold.

In the same field of endeavor, however, Pandula discloses phase cancellation sensor comprises a full wave rectifier plus integrator plus a sample and hold (column 1, lines 10 – 33, Fig. 1; wherein the phase cancellation sensor is interpreted as the phase detector, which produces the phase error signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Pandula, in the system of

Schneider because this would provide a means for adjusting the phase error, as disclosed by Pandula (column 1, lines 44 – 52).

22. Claims 23, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Bellenger (US 6,320,867).

Regarding claim 23, Schneider does not disclose that the master and then the slave are adjusted for amplitude and phase.

In the same field of endeavor, however, Bellenger discloses the state machine controls the amplitude and/or phase adjustment on power up or on request, sequentially, first the master and then the slave (Fig. 9; column 27, lines 59 – column 29, lines 3; wherein controlling the amplitude and phase are interpreted as training the echo canceller, on request is interpreted as when the call modem initiates the call, the master and slave are interpreted as the call modem and answer modem respectively and the state machine that determines the amplitude/phase is interpreted as modem processor). Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of Schneider because allowing the modems to train their echo cancellers, as is well know in the art.

Regarding claim 40, Schneider does not disclose a master/slave and that both are configured.

In the same field of endeavor, however, Bellenger discloses one of the circuits is a master die and another is a slave die, while the determining is repeated twice, first to configure the master die, and second to configure the slave die (Fig. 9; column 27, line 58 – column 29, line 3; wherein the master die and slave die are interpreted as the Call Modem and Answer Modem respectively).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of Schneider because this would allow the echo cancellers, of both master and slave, to be initialized during the training period, as is well known in the art.

23. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Bellenger (US 6,320,867) and Jensen (US 6,078,356).

Regarding claim 24, Schneider does not disclose that the amplitude cancellation sensor comprises an integrator plus a sample and hold device.

In the same field of endeavor, however, Jensen discloses that the amplitude cancellation sensor comprises an integrator plus a sample and hold device (column 4, lines 6 – 10; Fig. 2, elements 26, 60, 62).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Jensen, in the system of Schneider because this would provide a means for averaging the samples to reduce the effect of noise, as is well known in the art.

24. Claims 25, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Bellenger (US 6,320,867), Jensen (US 6,078,356) and Beall (US 3,988,686).

Regarding claim 25, Schneider does not disclose that the integrator includes a reset phase, an integration phase and a transfer phase.

In the same field of endeavor, however, Beall discloses the integrator includes a reset phase, an integration phase and a transfer phase (column 7, lines 7-28; wherein the transfer phase is interpreted as the dumping of the integration charge).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Beall, in the system of Schneider because this would provide a means clearing the integrator at the start of each integration phase, and then providing the output at the end of the integration phase, as is well known in the art.

Claim 29 is similarly analyzed as claim 25.

25. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Bellenger (US 6,320,867), Jensen (US 6,078,356), Beall (US 3,988,686) and Eisenberg (US 5,742,201).

Regarding claim 26, Schneider does not disclose that a control unit controls the timing of the phases.

In the same field of endeavor, however, Eisenberg discloses the timing of the phases for the phase cancellation sensor is controlled by the finite state machine (column 2, lines 5-9, 15 – 32; wherein the finite state machine is interpreted as the phase amplitude controller, controlling the timing is interpreted as being done by adjusting the phase adjustment control voltages, and the phase cancellation sensor is interpreted as the comparison that is done between the phase of the input and output signal, i.e. the comparison that produces the phase error)

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Eisenberg, in the system of Schneider because this would provide a means for using the phase error to adjust the phase timing, as is well known in feedback systems art.

26. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Sugawara (US 5,790,335).

Regarding claim 27, Schneider does not disclose training signals are injected into the transmitter to measure offsets.

In the same field of endeavor, however, Sugawara discloses patterns are injected into the transmitter for the purpose of measuring the offset in the amplitude cancellation sensor (column 7, lines 64 – column 8, line 7; column 14, lines 49 – 53; column 15, lines 20 – 23; wherein the pattern injected into the transmitter is interpreted as the data being injected into element 5 and the amplitude cancellation sensor is interpreted as the amplitude error detector 5).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Sugawara, in the system of Schneider because this would provide a means for measuring the offset, as disclose by Sugawara (column 14, lines 49 - 53).

27. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Eisenberg (US 5,742,201).

Regarding claim 30, Schneider does not disclose that a control unit controls the timing of the phases.

In the same field of endeavor, however, Eisenberg discloses the timing of the phases for the phase cancellation sensor is controlled by the finite state machine (column 2, lines 5-9, 15 – 32; wherein the finite state machine is interpreted as the phase amplitude controller, controlling the timing is interpreted as being done by adjusting the phase adjustment control voltages, and the phase cancellation sensor is interpreted as the comparison that is done between the phase of the input and output signal, i.e. the comparison that produces the phase error)

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Eisenberg, in the system of Schneider because this would provide a means for using the phase error to adjust the phase timing, as is well known in feedback systems art.

28. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Bellenger (US 6,320,867) and Minami et al. (US 4,977,551).

Regarding claim 32, Schneider does not disclose multiple patterns for purposes of offset calculation amplitude cancellation and phase calculation.

In the same field of endeavor, however, Bellenger discloses multiple patterns are selectable by the finite state machine for the purposes of offset calibration, amplitude cancellation and phase cancellation (column 24, line 52 – column 25, line 4; column 32, lines 48 – 59; wherein the multiple patterns are interpreted as the multiple training sequences during the 5 intervals, the finite state machine is interpreted as the DSP used to implement the negotiation, and the amplitude and phase cancellation is interpreted as setting up the echo channel parameters).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of Schneider because this would provide a means for training the echo canceller, as is well known in the art.

29. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Ramamurthy et al. (US 5,787,114).

Regarding claim 33, Schneider does not disclose looping the transmitted signal back to the receiver.

In the same field of endeavor, however, Ramamurthy discloses either the differential buffer or the output buffer of the transmitter is adapted to be switched off with the effect that the first signal is not canceled but is passed to the receiver for testing purposes

(column 5, lines 25 – 34; wherein the differential buffer being switched off is interpreted as being in the loop back mode, since it is well know in the art that in loop back mode, the feedback signal should not be cancelled).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Ramamurthy, in the system of Schneider because this would provide a means for testing the transmitted data, as is disclosed by Ramamurthy.

30. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Schulte et al. (US 5,726,592).

Regarding claim 34, Schneider does not disclose that N-type FET transistors are used.

In the same field of endeavor, however, Schulte discloses the load in the differential buffer providing the third signal is implemented as N-type FET transistors to minimize the parasitic capacitance (column 7, lines 35 – 39).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Schulte, in the system of Schneider because this would reduce the variance in receiver delay resulting in

changes in the input common-mode voltage level, as stated by Schulte (column 5, line 60 – column 6, line 4).

31. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984) and Blackwell (US 6,259,680).

Regarding claim 36, Schneider does not disclose that the phase of the echo replica is opposite to the phase of the leakage signal.

In the same field of endeavor, however, Blackwell discloses the phase of the third signal is shifted by opposite to the phase of the first signal (Fig. 2, inputs to element 324; column 7, lines 49 – 51; wherein the opposite phase of the two signals is interpreted as being the opposite signs of the subtractor 324).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Blackwell, in the system of Schneider because this would allow the echo to be cancelled, as is well known in the art.

32. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of

Ambrosio et al. (US 4,755,984) and Chang et al. (A CMOS Differential Buffer Amplifier with Accurate Gain and Clipping Control; July 1995, IEEE Journal of Solid State Circuits; pages 731 – 735).

Regarding claim 38, Schneider does not disclose that the gain of the differential buffer is varied by a training pattern.

In the same field of endeavor, however, Chang discloses the gain of the differential buffer is varied by means of a finite state machine (page 731, 2nd column, 6 lines starting with "However, for modern digital telephone applications, ..."; wherein the finite state machine that controls the gain is interpreted as the external gain control).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Chang, in the system of Schneider because allowing the gain to be externally controlled would allow greater flexibility, as is well known in the art.

33. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Adham et al. (US 6,100,716) and further in view of Ambrosio et al. (US 4,755,984), Bellenger (US 6,320,867) and Minami et al. (US 4,977,551).

Regarding claim 39, Schneider does not disclose that a training pattern is used to adjust the amplitude and phase of the echo replica, that peak error is minimized and that an ADC and DAC are used.

In the same field of endeavor, however, Minami discloses minimizing peak to peak noise by varying the codes in DACs, measuring noise using a peak detector and ADC to determine which code corresponds to the minimum noise using state machine and applying the determined code to the DACs at the end of adjustment process (column 2, lines 35 – 49; wherein the finite state machine is interpreted as the control unit).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Minami, in the system of Schneider because this would provide a means for adjusting the tracking signal (Minami; column 2, lines 30-31).

In the same field of endeavor, Bellenger discloses the phase and/or amplitude of the third signal is adjusted by applying a training pattern (column 27, lines 59 – column 29, line 3; wherein the third signal is interpreted as the echo replica, adjusting the phase/amplitude is interpreted obtaining the echo canceller coefficients using the training sequence).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of

Schneider because this would provide a means for training the echo canceller, as is well known in the art.

Other Prior Art Cited

34. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to echo cancellation and differential buffers/amplifiers:

Guidoux (US 4,621,173) discloses a method to reduce the convergence time of an echo canceller.

Ito et al. (US 5,450,457) discloses a sampling phase extracting circuit and echo canceller.

Mellado et al. (US 5,796,731) discloses multiline PCM interface for signal processing.

Shattil (US 20010019264) discloses a method and apparatus for a full-duplex electromagnetic transceiver

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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AD

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